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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,175	PORTERFIELD, A. KENT	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-15,22-29 and 37-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 27-29* is/are allowed.

6)☒ Claim(s) *1,2,4-6,9-11,22-26,37 and 40-59* is/are rejected.

7)☒ Claim(s) *7,8,12-14,38 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 7/05/2006

2. Claims 1-2, 4-15, 22-29, 37-59 are pending for examination.

3. The text of those sections of Title 35, U.S. code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by PCI Special Interest Group "PCI Bus Power Management Interface Specification" Rev. 11, December 18, 1998 ("Special").

6. As per claim 1, Special discloses an apparatus comprising:

a hardware linked list, the hardware linked list including a plurality of nodes, each of the plurality of nodes including a next node pointer register, wherein each of the plurality of nodes includes a register to specify a capability of the apparatus [Fig. 4 page 23].

Special does not explicitly teach a locking mechanism to conditionally make the next node pointer register of each of plurality of nodes read-only. However, this feature is deemed to be inherent to the Special system as section 3.2.2 page 25 show the next node pointer register of each of plurality of nodes is Read Only. The Special system would not able to lock the next

node pointer register of each of plurality of nodes if there is not a locking mechanism to perform the lock condition.

7. Claims 6, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Mitra et al. (Mitra) U.S. Patent 6,167,472.

8. As per claim 6, Mitra discloses a PCI local bus compliant device comprising:

a hardware implemented capabilities list [col. 1 lines 37-39, col. 2 lines 64-67] capable of being modified by low level software [col. 4 lines 25-33; col. 9 lines 31-35], and read-only to higher level software[1] [col. 2 lines 52-67], wherein a modification to the capabilities list by the low level software modifies capabilities from the PCI local bus compliant device [col. 4 lines 61-62; col. 9 lines 32-35].

Mitra does not explicitly teach a modification to the capabilities list by modifies capabilities available from the PCI device. However, this feature is deemed to be inherent to the Mitra system as lines 31-40 col. 9 show a configuration software running on the host device can modify or change a particular default configuration information value to a new configuration information value[2]. The Mitra system would be inoperative if the available new value was not supported by the PCI local bus compliant device.

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[1] As disclose by Mitra, in order to be identified during computer system startup, each PCI peripheral device is capable of reporting certain information referred as configuration information [col. 1 lines 32-39; col. 2 lines 52-59]. The configuration information typically includes parameters for indicating a vendor ID, serial number, base address register, and device capabilities [col. 2 lines 60-64]. Therefore, inherently the configuration information included a capabilities list.

Specifically, Mitra teaches, once the configuration software is able to communicate with the PCI peripheral device, the configuration software can modify the configuration information if necessary. In order to change a particular configuration information value (inherently included the capabilities list), the software stores a new data value in the corresponding memory location in the programmable non-volatile memory on the PCI peripheral device [col. 4 lines 25-33; col. 9 lines 32-35].

[2] Inherently, this modification included the modifying of a capability value.

9. As per claim 10, Mitra discloses the PCI local bus compliant device comprises an integrated circuit that includes the hardware implemented capabilities list [fig. 3]

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

12. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 1, 2, 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon U.S. Patent No. 5,925,134 in view of Sibigtroth.

14. As per claim 1, Solomon discloses an apparatus comprising:

a hardware linked list, the hardware linked list including a plurality of nodes, each of the plurality of nodes including a next node pointer register, wherein each of the plurality of nodes includes a register to specify a capability of the apparatus [col. 7 lines 22-26]; and

However, Solomon does not explicitly teach a locking mechanism to conditionally make the next node pointer register of each of plurality of nodes read-only.

Sibigtroth teaches another method related to a write protection circuit and method for a control register which allows a write protected register to be written only once [col. 1 lines 10-13]. Specifically, Sibigtroth teaches a locking mechanism to conditionally make the register read-only [fig. 3].

As taught by Sibigtroth, certain control registers and bits which determine system configuration would pose serious system integrity problems were they writeable, or under software control , during normal operation [col. 1 lines 14-17]. Therefore, it would have been obvious to one of ordinary skill in the art at time of the invention was made to have modified the system of Solomon with the lock mechanism of Sibigtroth to conditionally make the next node pointer register of each of the plurality of nodes read-only.

The motivation for doing so would have been to prevent accidental write or modification to the linked list structure since an unintended modification to these registers could change the device configuration/capability resulting in a device failure [col. 1 lines 18-21].

15. As per claim 2, Sibigtroth teaches the locking mechanism comprises a control register [110 fig. 3].

16. As per claim 4, Solomon teaches the apparatus comprises a PCI local bus compliant peripheral device [inherent – col. 7 lines 11-13].

17. As per claim 5, Solomon teaches the apparatus comprise an integrated circuit having a microprocessor bus compatible interface [inherent].

18. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mitra as applied to claim 6 above, and further in view of Gafken.

19. As per claim 9, Mitra does not explicitly teach the hardware implemented capabilities list is writeable by basic input output software and read-only to operating system software.

However, Mitra explicitly teaches that the hardware implemented capabilities list is writeable by any software. Therefore, it is obvious to one of ordinary skill in the art that the generic software of Mitra encompasses the claimed basic input/output software since the particular software does not alter the Mitra system.

and inherently, Mitra teaches the implemented capabilities list is read-only to operating system software.

20. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen et al. U.S. Patent 6,154,819 in view of Special.

21. As per claim 11, Larsen et al. teach an integrated circuit comprising:

an address bus [inherent – fig. 1, 7];

a data bus [inherent – fig. 1, 7];

a control bus [fig. 2, 3];

a series of memory array blocks coupled to the address, data, and control busses, the series of memory array blocks arranged in a writeable list [col. 1 lines 37-40; 202 fig. 2];

a control register [116, 206 fig. 2] operable to lock the writeable memory array blocks and conditionally make the series of memory blocks read-only [col. 4 lines 12-16; col. 7 lines 37-53]; and

wherein the control register is writable only by a first level of software[3] [204 fig. 2; col. 6 lines 48-63] and the series of memory array blocks are inherently accessible by a second level of software [col. 11 lines 45-51].

However, Larsen et al. do not teach the memory array blocks are arranged as a linked list.

Special teaches another integrated circuit having a storage spaces for storing the device's capabilities. Specifically, Special teaches the storages spaces arranged in a series of linked list registers [Fig. 4 page 23].

At the time of the invention was made, it would have been obvious a person of ordinary skill in the art to have modified the system of Larsen et al. with a linked list data structure as taught by Special since Larsen et al. do not explicitly prohibit the use of linked list and linked list, which allows for rapid insertion and removal of the elements in the linked list without having to move or relocate large blocks of physical memory, is such a well know data structure for storing information.

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[3] First level-software or low-level software by definition is a software which handles the interface to peripheral hardware. As teach by Larsen et al. in col. 6 lines 45-48, a locked down block can only be unlocked by a device reset or thought the use of a special hardware override pin. Therefore, inherently Larsen et al. teach the control register is writeable only by a first level of software.

22. Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon in view of DeRoo et al. U.S. Patent 5,764,995.

23. As per claim 22, Solomon teaches an integrated circuit comprising:

a first register to signify whether a capabilities list is enabled [col. 7 lines 20-22];

a second register to point to a capabilities list [col. 7 lines 22-29];

However, Solomon does not explicitly teach a first and second register as a writeable register and a write-once control register operable to make the first and second writeable register read-only.

DeRoo et al. teach another integrated circuit comprising plurality of writeable registers for storing plurality of configuration [col. 2 lines 28-34]. Specifically, DeRoo et al. teach a write-once control register operable to make the plurality of writeable register read-only [claim 1; col. 2 lines 39-47].

At the time of the invention was make, it would have been obvious to one of ordinary skill in the art to have modified to system of Solomon with a writeable register and a write once control register of DeRoo et al. to make the first and second writeable registers read-only.

The motivation for doing so would have been to provide the system the ability to modify/reprogram the specific configuration in the registers without having manually reconfigured [from col. 1 line 60 to col. 2 line 26] and prevent unintended erasure during the normal operation of the system.

24. As per claim 23, DeRoo et al. teach the control register can be written only once between system resets [claim 1].

25. As per claim 24, Solomon teaches a hardware linked list pointed to by the second writeable register, the hardware linked list including a plurality of nodes [col. 7 lines 20-24]. And DeRoo et al. teach a writeable register to provide the system the ability to reprogram the specific information in the register.

26. As per claim 25, the combine teaching of Solomon and DeRoo et al. inherently teach the control register operable to make the writeable next node register read-only.

27. As per claim 26, Solomon teaches a PCI local bus compliant interface [col. 7 lines 11-13].

28. Claims 37, 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon in view of Larsen et al.

29. As per claim 37, Solomon teaches a computer system comprising:

a PCI local bus compliant peripheral device coupled to a bus [121, 122 fig. 1]; and

a processor [101 fig. 1] coupled to the bus;

wherein the PCI local compliant peripheral device includes a capabilities linked list assessable by the processor[col. 7 lines 22-26].

However, Solomon does not explicitly that the capabilities linked list is modifiable by the processor, and wherein the PCI local bus compliant peripheral device further includes a writeable control register operable to render the capabilities linked list read-only by the processor.

Larsen et al. teach another device comprises a serious of writeable memory array usable to store upgradeable configuration information [col. 1 lines 39-41] wherein the serious of register [202 fig. 2] coupled to the address, data [fig. 7], and control busses [fig. 3]. Specifically, Larsen et al. teach a control register [col. 4 lines 14-16, 56-67] operable to lock the writeable series of writeable memory array and conditionally make the series of lined list register read-only [abstract, col. 7 lines 33-54] by the processor.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to have modified the system of Riley et al. with a series of writeable register (memory array) and a control register operable to lock and conditionally make the serious of register read-only as taught by Larsen et al.

The motivation for doing so would have been to provide the system the ability to upgrade or reprogram the information stored in the plurality of the registers; and at the same time, protect the information from unintended erasure or reprogramming as teach by Larsen et al. [col. 1 lines 39-43; 56-59; col. 2 lines 62-65].

30. As per claim 40, Larsen et al. teach a memory device having processor instructions stored therein, the processor instructions being operable to cause the processor to write to the writeable control register [from col. 3 line 62 to col. 4 line 11; col. 7 lines 37-41].

31. As per claim 41, Solomon teaches the PCI local bus compliant peripheral device includes register to indicate whether the capabilities linked list is enabled [col. 7 lines 20-22]. However, Solomon does not explicitly teach that the register is writeable. Larsen et al teach a

programmable series of memory array blocks such that it would have been obvious to one of ordinary skill in the art that the combine teachings of Solomon and Larsen et al. included the claimed writeable register.

32. Claims 42-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon in view of Gafken U.S. Patent 6,026,016.

33. As per claim 42, Solomon teaches a hardware linked list comprising:

a first list node having a capabilities register and a next node pointer register; and

a second list node having a capabilities register and a next node pointer register [col. 7 lines 22-34];

Solomon does not teach a control register, and in response to the control register, the next node pointer registers of the first and second list nodes are conditionally read-only.

Gafken teaches a method for controlling locking and unlocking of a block in a memory array. Specifically, Gafken teaches a control register [137, 135, 140 fig. 1] and wherein the plurality of blocks in the memory array are conditionally made read-only in response to the control register [col. 6 lines 38-44].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Solomon with the control register of Gafken to conditionally made the next node pointer registers of the first and second list nodes read-only.

The motivation for doing so would have been to prevent inadvertent overwriting or other undesired alteration to the linked list which would compromise the device integrity.

34. As per claim 43, Solomon teaches a head pointer register to point to the first list node and Gafken teaches a writeable register wherein the writeable register are conditionally read-only in response to the control register. Therefore, it is obvious to one of ordinary skill in the art that the combine teachings of Solomon and Gafken teach the writeable head pointer register being conditionally read-only in response to the control register.

35. As per claim 44, Solomon teaches the hardware linked list is compliant with a PCI local bus rev. 2.2 capabilities list [col. 40 line 42].

36. As per claim 45, Gafken teaches the control register is a write-once register [from col. 7 line 64 to col. 8 line 5].

37. As per claim 46, Gafken teaches the control register can be written to only once between hardware resets [see claim 45; col. 10 lines 47-52].

38. As per claim 47, Solomon teach a method of initializing a computer peripheral comprising:

during initialization of the computer peripheral, the computer system communicates with the peripheral to obtain a list of capabilities stored in a hardware linked list within the peripheral [col. 7 lines 24-26].

Solomon does not expressly teach the writing a list of capabilities to nodes in a hardware linked list. Particularly, Solomon does not teach that the system have the ability to modify the linked list or teach a control register within the computer peripheral to made the nodes read-only.

Gafken presented another invention relates generally to a memory array and more particularly to a method and apparatus for locking and unlocking blocks of memory cells in a nonvolatile memory array to disable and enable write and erase. Specifically, Gafken teaches due to the nature of the locking mechanism of previous art, in order to update or make modification to the critical information in the memory, the user required to open up the system to physically change the setting to unlock the memory. Therefore, while system critical information is protected in locked blocks, updates to such information can be difficult.

Gafken teaches, during the initialization of the computer peripheral [115 fig. 3-memory module], the writing/re-programming of the desired location in the memory array [515 fig. 5; col. 13 lines 59-65] and to a control register [315 fig. 3] within the computer peripheral to make the location of memory array read-only [from col. 13 line 66-3].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Solomon with the ability to modified the location of memory array [register] of Gafken to write a list of capabilities to nodes in a hardware linked list and a control register taught by Gafken to make the nodes read-only.

The motivation for doing so would have been to provide the system the ease of use and upgradeability of the list of capabilities to node in a hardware linked list; and at the same time, to prevent inadvertent erasure or modification to the linked list.

39. As per claim 48, Gafken teaches the method for altering the information a desire location of the memory. Therefore, it is obvious to one of ordinary skill in the art that the combine teachings of Solomon and Gafken teach the modifying to the next node pointer register.

40. As per claim 49, Gafken teach writing to a control register comprises writing once to a capabilities lock bit, which thereafter is read-only [see claim 45-46].

41. As per claim 50, Solomon teaches a capabilities list enabled register [col. 7 lines 20-21] and Gafken teaches the system with the ability to modify a read-only register. Therefore, it is obvious to one of ordinary skill in the art that the combine teaching of Solomon and Gafken teach the writing to a capabilities list enabled register.

42. As per claim 51, Gafken teaches the method is performed by basic input output software prior to loading of an operating system [fig. 5]

43. As per claim 52, Solomon teaches a method of initializing a PCI local bus compliant device comprising:

reading a link within a capabilities linked list in the PCI local bus compliant device. However, Solomon does not teach reading instructions from a memory device holding basic input output software to modify a link within a capabilities linked list and writing to a control register in the PCI local bus compliant device to make the link read-only.

Gafken present another invention relates generally to a memory array and more particularly to a method and apparatus for locking and unlocking blocks of memory cells in a

nonvolatile memory array to disable and enable write and erase. Specifically, Gafken teaches due to the nature of the locking mechanism of previous art, in order to update or make modification to the critical information in the memory, the user required to open up the system to physically change the setting to unlock the memory. Therefore, while system critical information is protected in locked blocks, updates to such information can be difficult.

Gafken teaches, during the system initialization, reading instruction from a memory device holding basic input output software [151 fig. 1; col. 13 lines 26-40];

modifying a desired locations in the memory array within the memory module[col. 13 lines 62-63]; and

writing to a control register in the memory module to make the location in the memory array read-only [from col. 13 line 66 to col. 14 line 2].

At the time of the invention was make, it would have been obvious to one of ordinary skill in the art to have modified to system of Solomon with the reading instruction from a memory device holding BIOS software as taught by Gafken to modify a link within a capabilities linked list in the PCI local bus compliant device in the Solomon system and a control register taught by Gafken to make the link read-only,

The motivation for doing so would have been to provide ease of use and upgradeability of the link within the linked list; and at the same time, to prevent inadvertent erasure or modification to the linked list [col. 14 lines 27-40].

44. As per claim 53, the examiner takes Official Notice of the fact that the manipulation of the linked list is an old and well-know method.

45. As per claim 54-55, Gafken teaches the system with the ability to modify a read-only register. Therefore, it is obvious to one of ordinary skill in the art that the combine teaching of Solomon and Gafken teach the writing to a capabilities list enabled register and to a head pointer register in order to modify the capabilities list.

46. As per claim 56, Solomon teach an apparatus having a computer readable medium with machine-readable instructions for a method stored thereon, the method comprising:

reading a next node pointer register in a PCI local bus peripheral to indicate the existence of a capability [col. 7 lines 20-22].

However, Solomon does not teach the modifying a next node pointer register or a control register to make the next node pointer register read-only.

Gafken teach another method for modifying a location in a memory [register]; and

the modifying a control register to make the next node pointer register read-only [see discussion in claim 52].

47. As per claim 57, Solomon teaches a head pointer register to point to a hardware linked list. Gafken teaches the system with the ability to modify a protected register and, after modify, re-lock the register to render the register read-only responsive to the control register. Therefore, it is obvious to one of ordinary skill in the art that the combine teaching of Solomon and Gafken teach the modifying of a head pointer register to a hardware capabilities linked list, wherein the head pointer become read-only responsive to the control register.

48. As per claim 58, Gafken teach the apparatus comprises a read-only memory [abs]

49. As per claim 59, see claim 50.

Allowable Subject Matter

50. Claims 15, 27-29 are allowed.

51. Claims 7-8, 12-14, 38-39 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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